IT-μDTC firmware development
Simulation and testing of RD53A Chip Readout with FC7

Tamás Balázs, Viktor Veszprémi
MTA Wigner RCP

Nov 30, 2018

Supported by OTKA K124850
IT-µDTC Firmware Development Update

- Running development tasks in order
  → Porting DIO5 → **Ready**
  → Porting TLU → **Ready**
    → i2c multi-master problem with CERN, KSU and DIO5 FMCs → **need to be solved**...
  → Porting TTC Decoder → **To do**...
  → Porting AMC13 → **To do**...

**I2C multi-master problem**

- Overview and possible solutions
  → CERN and KSU FMCs need the same state machines
  → DIO5 has different state machine, it feeds the i2c slave with writing a FIFO through IPBus registers
  → we can try to use the i2c master in system core which has IPBus integration
  → or we can use i2c master core from Opencores which supports multi-master operations

**Testing aurora_rx with KSU FMC**

- Overview and summary
  → 1 lane aurora_rx tested in L12 FMC on J7 connector
  → aurora_rx tested by Russell in L12 FMC on J2 connector
IT-μDTC Firmware Development Update

Modifications on CERN FMC

- Past and current changes
  - C18 and C19 have already bypassed to have DC coupled clock
  - both in version 1 and 2 boards C34 and D35 pulled to GND
  - in L8 FMC this GND point is pulled up to 3.3V!
  - vias are located under the FMC connector
  - easiest solution is to remove electrical contacts from the FMC connector in CERN FMC
  - all functionalities remain the same

Testing aurora_rx with CERN FMC

- Overview and current state of testing
  - gtx reference clock constraint modified according to L8 FMC
  - 1 lane aurora_rx reconfigured to X0Y7 gtx
  - in case of L8 FMC gtx differential signal polarity is reversed
  - so far gtx locked to PLL but aurora_rx lane and channel up did not go high