Trigger and Clock distribution for IT/OT μDTC

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Supported by OTKA K124850
→ µTCA crate control via MCH
→ TTC FC7 → DIO5 in L8 (needs to be in order to input ext-clock)
→ 8SFP FMC in L12 (spec FMC, SFP routed to select I/O)
→ AMC13 → AMC13 receives TTC signal (L1A, EC0, BC0, CLK 160MHz) from TTC FC7
→ distributes FCLKA + L1A on backplane
→ IT/OT µDTC → reads/controls IT/OT modules, receives clock + L1A in backplane
Steps for IT/OT µDTC

1) port AMC13/TTC decoder/TLU/DIO5 blocks to IT-µDTC
2) test IT/OT receives clock from AMC13
   → event counter in be_proc → did not count L1As
   → took AMC13 to Budapest for debugging
   → successfully set up AMC13, sent periodic triggers
   → traced signal in backplane with oscilloscope
   → in fabric with chipscope (IDDR, channel_a/channel_b, TTC out port)
   → now see bc0/ec0/l1a in TTC output
   → event counter counts if fast command block bypassed
      TO DO: debug fast command block

Note: → verified in AMC13 loopback that TTC decoder / amc13 blocks ported correctly
      TO DO: ready to test clock + trigger from TTC FC7
L1A triggers detected in FC7
Steps for TTC FC7

→ DIO5 In L8
  → testing already done sometime ago
  → DIO5 reads I/O channels, selectable direction, thresholding is possible
  → configured by i2c master and tested via oscilloscope
  → must be in L8 so that external clock can be routed into fabric

→ 8SFP FMC in L12
  → got the right one during last DAQ school
  → constraints ready, know how to program by i2c
  → **TO DO:** i2c needs to be integrated and sending clock to AMC13 tested

→ TTC FC7 simple firmware written in summer
  → can send clock or clock + L1A
  → control by python
  → little tested
  → L1A counter and sending EC0 needs to be implemented
Summary

→ IT μDTC fast command block needs check
→ 8SFP FMC i2c programming in progress
→ test TTC firmware in FC7